International Journal of Electrical, Electronics and Computer Engineering **1**(2): 60-64(2012)

ISSN No. (Online) : 2277-2626

Design of Wimax Interleaver using Finite State Machine

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(Received 30 October, 2012, Accepted 17, November, 2012)

ABSTRACT: OFDM is multiplexing technique used in WiMAX standards as it is always challenging to find FPGA solution because of its area and operating frequency. We have developed Interleaver which plays a vital role in improving the performance of FEC (Forward Error Correction Codes) codes in terms of Bit Error Rate over wireless channel. The proposed work justify the efficient structure for interleaver by address generation using FSM and data path control i.e. interaction with memory using multiplexers. The interleaver design with the integrated PRBS is developed using VHDL. The implementation of PRBS generator is based on the linear feedback shift register, which consists of 'n' master slave flip-flops. The PRBS generator produces a predefined sequence of 1's and 0's, with 1 and 0 occurring with the same probability.

Keywords: Interleaver, WiMAX, FSM, FEC, FPGA, PRBS.

I. INTRODUCTION

WIMAX (Worldwide Interoperability for Microwave Access) technology is a telecommunications technology that offers transmission of wireless data via a number of transmission methods; such as portable or fully mobile internet access via point to multipoint links.

WIMAX forum promises to offer high data rate over large areas to a large number of users where broadband is unavailable. This is the first industry wide standard that can be used for fixed wireless access with substantially higher bandwidth than most cellular networks [1]. Wireless broadband systems have been in use for many years, but the development of this standard enables economy of scale that can bring down the cost of equipment, ensure interoperability, and reduce investment risk for operators.

This paper is useful for analysis of physical layer of WIMAX with different modulation techniques like BPSK, QPSK, QAM and comparison of QPSK modulation with and without Forward Error Correction methods. Broadband Wireless Access (BWA) has emerged as a promising solution for last mile access technology to provide high speed internet access in the residential as well as small and medium sized enterprise sectors[3]. At this moment, cable and digital subscriber line (DSL) technologies are providing broadband service in this sectors.

The IEEE 802.16e standard specified OFDM as the transmission method. The OFDM signal is made up of many orthogonal carriers, and each individual carrier is digitally modulated with a relatively slow symbol rate. This method has distinct advantages in multipath propagation because, in comparison with the single carrier method at the same transmission rate, more time is needed to transmit a symbol.

II. SYSTEM MODEL

A. WIMAX Address Generator

The VHDL model of the address generator for OFDM based WIMAX is prepared using Xilinx Integrated Software Environment (ISE) and is implemented on Xilinx spartan-3 (Device: XC3S400) FPGA platform [4].

B. Interleaver

Interleaver is mainly used to correct burst error. After puncturing process the data is passed through the interleaver. The main purpose to use it to minimizing burst error[8]. Interleaving is normally implemented by using a two-dimensional array buffer, such that the data enters the buffer in rows, which specify the number of interleaving levels, and then, it is read out in columns. The result is that a burst of errors in the channel after interleaving becomes in few scarcely spaced single symbol errors, which are more easily correctable.

WIMAX uses an interleaver that combines data using 12 interleaving levels. The effect of this process can be understood as a spreading of the bits of the different symbols, which are combined to get new symbols, with the same size but with rearranged bits.

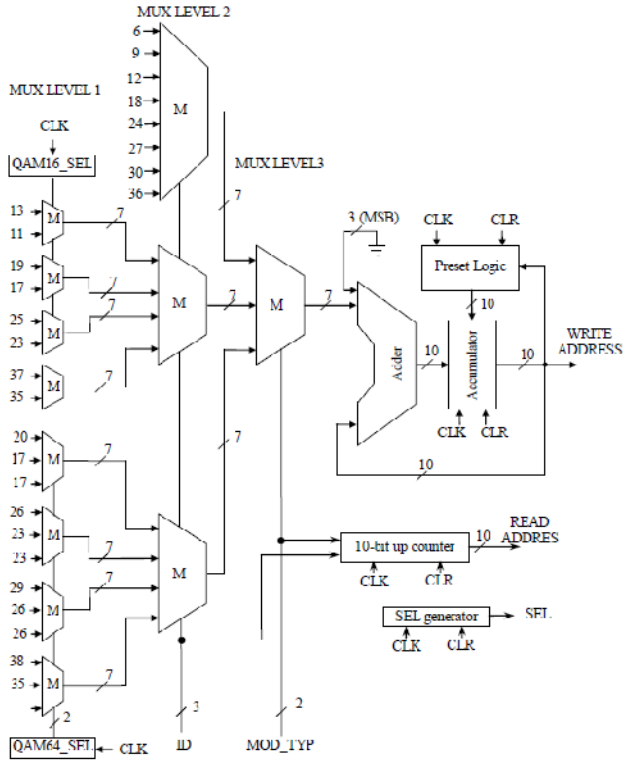

Fig. 1. WiMAX Address generator.

Encoded data are interleaved by a block interleaver. The size of the block is depended on the numbers of bit encoded per sub channel in one OFDM symbol, Ncbps. In IEEE 802.16, the interleaver is defined by two step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second permutation ensures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of unreliable bits.

The Interleaver is defined by a two-step permutation. The first ensures that adjacent coded bits are mapped onto nonadjacent subcarriers [2]. The second permutation ensures that adjacent coded bits are mapped alternately onto less or more significant bits of the constellation, thus avoiding long runs of lowly reliable bits, d represents number of columns of the block Interleaver which is typically chosen to be 16. mk is the output after first level of permutation and k varies from 0 to Ncbps -1. S is a parameter defined as s= max {1, Ncpc/2}, where Ncpc is the number of coded bits per subcarrier.

$$m_k = \left[\frac{N_{cbps}}{d}\right](k \,\%\, d) + \left[\frac{k}{d}\right]$$

$$j_k = s\times \left[\frac{m_k}{s}\right] + \left[m_k + N_{cbps} - \left(\frac{d\times m_k}{N_{cbps}}\right)\right]\% \, s$$

Where % is signify modulo function.

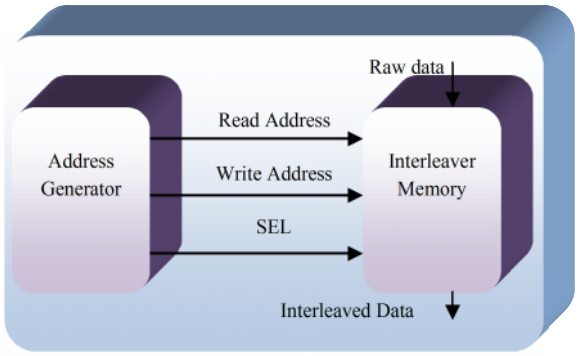

Fig. 2. Top level View of WIMAX Interleaver.

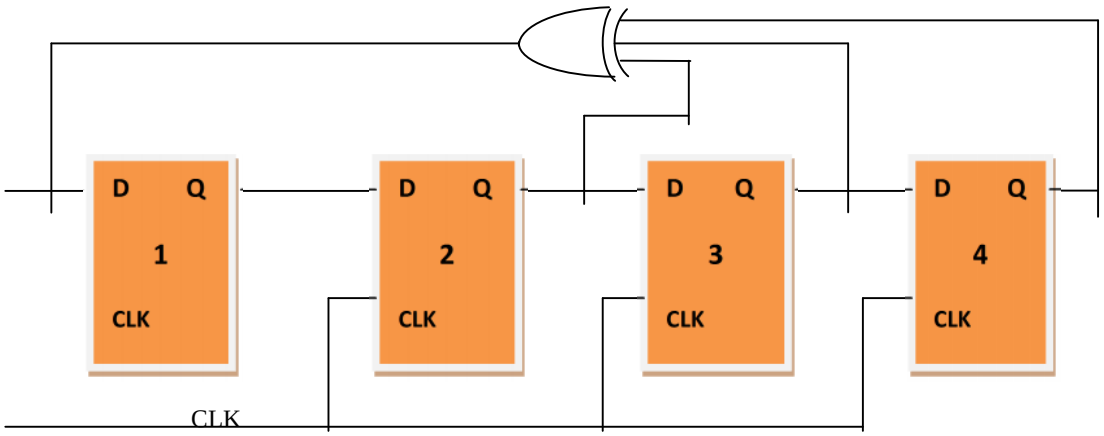

Fig. 3. Logic Diagram of Pseudo Random Binary Sequence Generator.

The modulation schemes generally used in the downlink and uplink are binary phase shift keying,quaternary phase shift keying,16-quadrature amplitude modulation, and 64-QAM [10].

1. *Multiplexer*: In our proposed architecture multiplexer is used for passing various control data and information to the destination

2. Accumulator: It takes data from adder and FSM (finite state machine) and latch it and transfer it to the next processing block according to the control signal.

3. FSM: It is a Mealy machine implementation of control statements which controls the address generation for interleaver according to the modulation technique. The preset logic block is the main control unit to generate the address of interleaver. Mealy machine has been implemented, taking consider of area efficiency. A counter is designed to take care of various address transition in a given state. There are 4 states according to modulation scheme selection. S_0 state works for zero selection, S_1 state works for one selection, S_0 state works for two selections and S3 is the idle state which works as a default state. The state transaction depends upon modulation type selection.

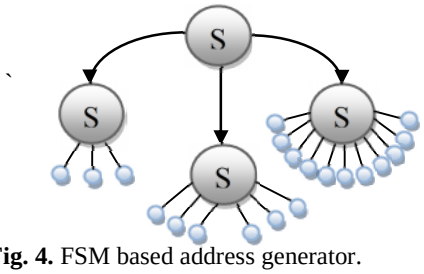

Fig. 4. FSM based address generator.

4. *Counter:* It is an up counter which keeps track of address generation during a specified state.

5. *RAM:* It is a storage element for the address which has been generated from FSM

6. *Inverter:* It inverts the control signal for multiplexer selection.

Table1: Write addresses for QPSK modulation scheme (Ncbps = 96).

0	6	12	18	24	30	36	42
48	54	60	66	72	78	84	90
1	7	13	19	25	31	37	43
49	55	61	67	73	79	85	91
2	8	14	20	26	32	38	44
50	56	62	68	74	80	86	92
3	9	15	21	27	33	39	45
51	57	63	69	75	81	87	93
4	10	16	22	28	34	40	46
52	58	64	70	76	82	88	94
5	11	17	23	29	35	41	47
53	59	65	71	77	83	89	95

7. *PRBS Generator:* PRBS or Pseudo Random Binary Sequence is essentially a random sequence of binary numbers. It is random in a sense that the value of an element of the sequence is independent of the values of any of the other elements.

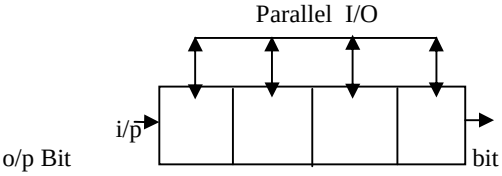

Fig. 5. Shift Register.

III. Simulation Results

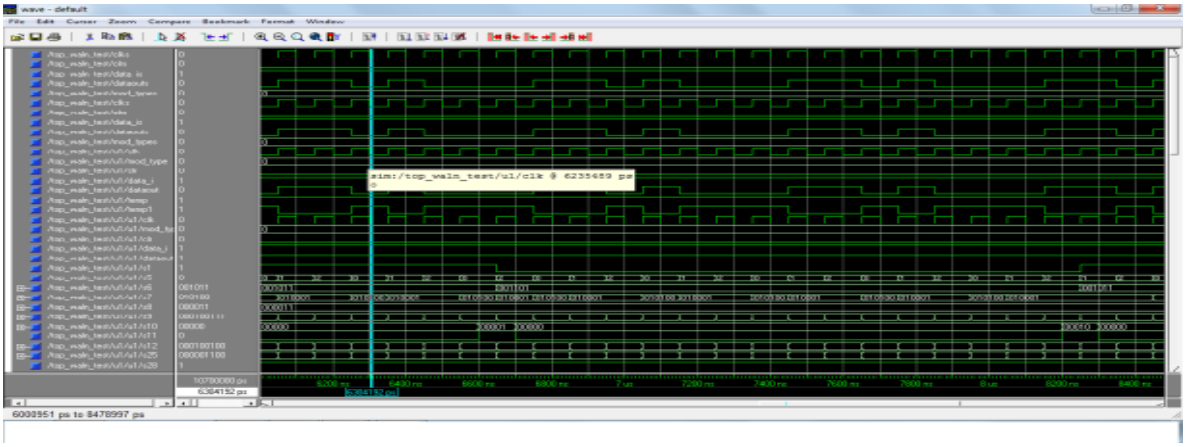

Fig. 6. Simulation waveform for QPSK modulation scheme with integrated PRBS (Ncbps = 96).

Fig. 7. Simulation waveform for QPSK modulation scheme with integrated PRBS (Ncbps = 96).

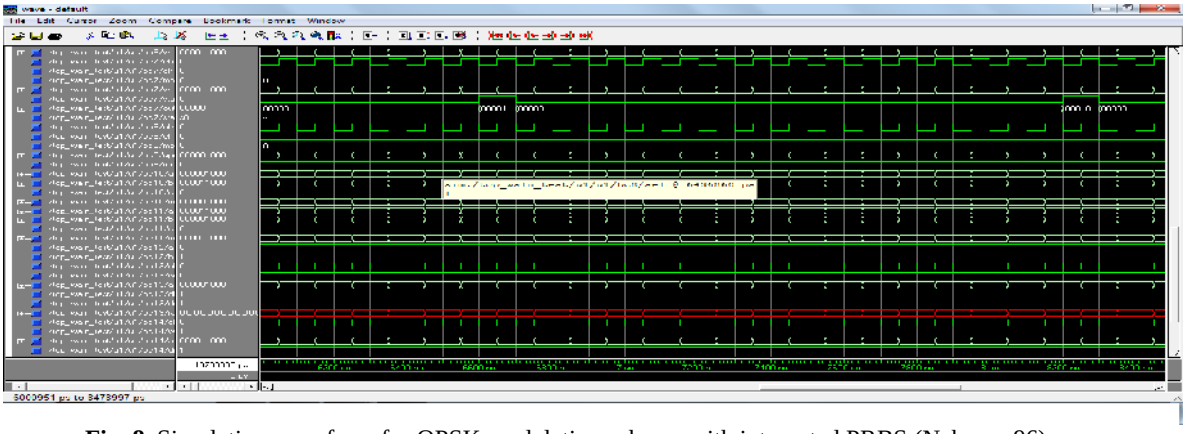

Fig. 8. Simulation waveform for QPSK modulation scheme with integrated PRBS (Ncbps = 96).

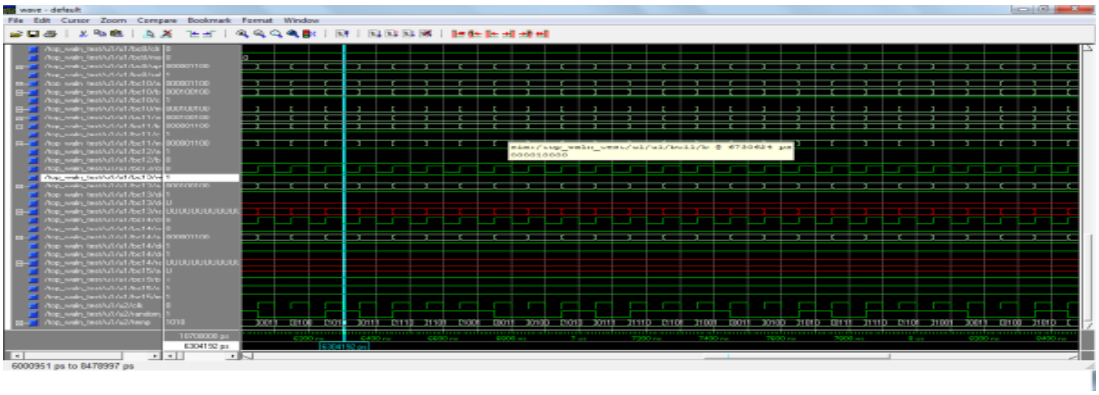

Fig. 9. Simulation waveform for QPSK modulation scheme with integrated PRBS (Ncbps = 96).

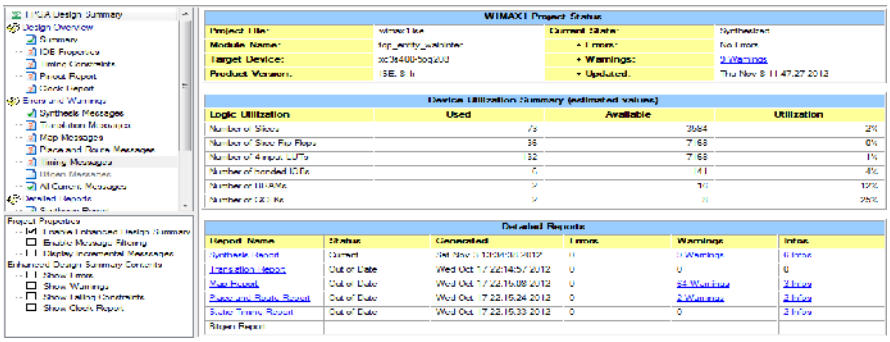

Fig. 10. Design summary of Interleaver.

IV. CONCLUSION

The complete interleaver has been divided into two sub modules; address generator and RAM. Address generator is implemented by Mealy machine and design has been tested by Modelsim. For FPGA implementation design has been synthesised on Xilinx ISE, Spartan 3 device. We found our designed has used 96 slices including memory element. A 16-bit PRBS is realized by shifting the input through the D-flip flops and feed backing the outputs of some registers known as taps again into the first register after passing them through a XOR gate. The process of realizing LFSR is carried out by first developing the VHDL code for a D-flip flop.

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